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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,936	09/09/2003	Richard M. Fastow	AMD-H0561	3102

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EXAMINER	
NGUYEN, DAO H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,936	FASTOW ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7,8,10,12,13 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,8,10,12,13 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 11/18/2005.

Claims 1, 7, 8, 10, 12, 13, and 21-25 are active in this application.

Claim(s) 2-6, 9, 11, and 14-20 have been cancelled.

Remarks

2. Applicant's arguments filed on 11/18/2005 have been fully considered, but are moot in view of the new ground of rejection(s).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 7, 8, 10, 12, 13, and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,693,321 to Zheng et al.

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Zheng discloses a flash memory cell, as shown in fig. 1, comprising:

a substrate 12 comprising a source 14 and a drain 16;

a silicon dioxide layer 20 adjoining said substrate 12;

a polysilicon floating gate 18:

a dielectric layer sandwiched between and adjoining both said silicon dioxide layer and said floating gate, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide (col. 7, lines 7-14 teaches that the gate dielectric 20 could be a multi-layer dielectric, and may be made of suitable gate dielectric materials including SiO_2 or of dielectric materials having a dielectric constant greater than SiO_2; therefore, gate dielectric layer 20 clearly can comprise two layers having dielectric constant greater than that of SiO_2; or alternately, gate dielectric layer 20 can definitely comprise a SiO_2 layer on the substrate and another layer formed on the SiO_2 layer and having dielectric constant greater than that of SiO_2; or alternately,

gate dielectric layer 20 can definitely comprise multi-layer dielectric made of SiO_2 and/or other suitable gate dielectric materials having a dielectric constant greater than SiO_2);

an oxide-nitride-oxide (ONO) layer 24 (col. 6, lines 15-31; and col. 7, lines 19-35) adjoining said floating gate 18; and

a control gate 32 adjoining said ONO layer 24.

Regarding claim 7, Zheng discloses the flash memory cell wherein said dielectric material comprises a metal oxide. See col. 7, lines 7-14 and Table 1.

Regarding claim 8, Zheng discloses the flash memory cell wherein said dielectric layer comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 7, lines 7-14 and Table 1.

Regarding claim 10, Zheng discloses a flash memory array, as shown in fig. 1, comprising memory cells, wherein a memory cell comprises:

a substrate 12 comprising a source 14 and a drain 16;

a first layer 20 comprising a silicon material: a tunnel oxide layer 20 sandwiched between and adjoining both said substrate and said first layer, said tunnel oxide layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide (col. 7, lines 7-14 teaches that the gate dielectric 20 could be a multi-layer dielectric, and may be made of suitable gate dielectric materials including SiO_2 or of

dielectric materials having a dielectric constant greater than SiO_2. Therefore, gate dielectric layer 20 clearly can comprise two layers having dielectric constant greater than that of SiO_2; or alternately, gate dielectric layer 20 can definitely comprise a SiO_2 layer on the substrate and another layer formed on the SiO_2 layer and having dielectric constant greater than that of SiO_2; or alternately, gate dielectric layer 20 can definitely comprise multi-layer dielectric made of SiO_2 and/or other suitable gate dielectric materials having a dielectric constant greater than SiO_2);

a polysilicon floating gate 18 adjoining said first layer;

an oxide-nitride-oxide (ONO) layer 24 (col. 6, lines 15-31; and col. 7, lines 19-35) adjoining said floating gate 18; and

a control gate 32 adjoining said ONO layer 24.

Regarding claim 12, Zheng discloses the flash memory array wherein said silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 7, lines 7-14 and Table 1.

Regarding claim 13, Zheng discloses the flash memory array wherein said dielectric material comprises a metal oxide. See col. 7, lines 7-14 and Table 1.

Regarding claim 21, Zheng discloses a flash memory cell, as shown in fig. 1, comprising:

a substrate 12 comprising a source 14 and a drain 16;

a first layer 20 comprising a first silicon material and adjoining said substrate 12; a second layer 20 comprising a second silicon material; a dielectric layer 20 sandwiched between and adjoining both said first layer and said second laver, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide (col. 7, lines 7-14 teaches that the gate dielectric 20 could be a multi-layer dielectric, and may be made of suitable gate dielectric materials including SiO_2 or of dielectric materials having a dielectric constant greater than SiO_2. Therefore, gate dielectric layer 20 clearly can comprise three layers having dielectric constant greater than that of SiO_2; or alternately, gate dielectric layer 20 can definitely comprise a SiO_2 layer on the substrate and another layer formed on the SiO_2 layer and having dielectric constant greater than that of SiO_2; or alternately, gate dielectric layer 20 can definitely comprise multi-layer dielectric made of SiO_2 and/or other suitable gate dielectric materials having a dielectric constant greater than SiO_2, for example, gate dielectric layer 20 can be an ONO layer) ;

a polysilicon floating gate adjoining said second laver;

an oxide-nitride-oxide (ONO) layer adjoining said floating gate; and

a control gate adjoining said ONO layer.

Regarding claim 22, Zheng discloses the flash memory cell wherein said first silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 7, lines 7-14 and Table 1.

Regarding claim 23, Zhend discloses the flash memory cell wherein said second silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 7, lines 7-14 and Table 1.

Regarding claim 24, Zheng discloses the flash memory cell wherein said dielectric material comprises a metal oxide. See col. 7, lines 7-14 and Table 1.

Regarding claim 25, Zheng discloses the flash memory cell wherein said dielectric layer comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 7, lines 7-14 and Table 1.

5. Claims 1, 7, 8, 10, 12, 13, and 21-25 rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,872,972 to Huang et al.

Regarding claim 1, Huang discloses a flash memory cell, as shown in figs. 2-6, comprising:

a substrate 404 comprising a source 404B and a drain 404A;

a silicon dioxide layer (lower dioxide layer in the ONO layer 420) adjoining said substrate 404;

a polysilicon floating gate 406:

a dielectric layer (upper nitride/oxide layer in the ONO layer 420) sandwiched between and adjoining both said silicon dioxide layer and said floating gate 406, said

dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide See col. 2, lines 9-16; col. 3, line 64 to col. 4, line 13;

an oxide-nitride-oxide (ONO) layer 422 adjoining said floating gate 406; and

a control gate 424 adjoining said ONO layer 422.

Regarding claim 7, Huang discloses the flash memory cell wherein said dielectric material comprises a metal oxide. See col. 3, line 64 to col. 4, line 13.

Regarding claim 8, Huang discloses the flash memory cell wherein said dielectric layer comprises a composite of a metal oxide and a material selected from the group

consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 2, lines 9-16; col. 3, line 64 to col. 4, line 13.

Regarding claim 10, Huang discloses a flash memory array, as shown in figs. 2-6, comprising memory cells, wherein a memory cell comprises:

a substrate 404 comprising a source 404B and a drain 404A;

a first layer (upper oxide layer in the ONO layer 420) comprising a silicon material:

a tunnel oxide layer (lower oxide/nitride layer in the ONO layer 420) sandwiched between and adjoining both said substrate 404 and said first laver, said tunnel oxide layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide (col. 2, lines 9-16; col. 3, line 64 to col. 4, line 13);

a polysilicon floating gate 406 adjoining said first layer;

an oxide-nitride-oxide (ONO) layer 422 adjoining said floating gate 406; and

a control gate 424 adjoining said ONO layer 422.

Regarding claim 12, Huang discloses the flash memory array wherein said silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 2, lines 9-16; col. 3, line 64 to col. 4, line 13.

Regarding claim 13, Huang discloses the flash memory array wherein said dielectric material comprises a metal oxide. See col. 2, lines 9-16; col. 3, line 64 to col. 4, line 13.

Regarding claim 21, Huang discloses a flash memory cell, as shown in figs. 2-6, comprising:

a substrate 404 comprising a source 404B and a drain 404A;

a first layer comprising a first silicon material (lower silicon oxide layer in the ONO layer 420) and adjoining said substrate 404;

a second layer comprising a second silicon material (upper silicon oxide layer in the ONO layer 420);

a dielectric layer (silicon nitride layer in the ONO layer 420) sandwiched between and adjoining both said first layer and said second laver, said dielectric layer comprising

a dielectric material (silicon nitride) having a dielectric constant greater than that of silicon dioxide;

a polysilicon floating gate 406 adjoining said second laver;

an oxide-nitride-oxide (ONO) layer 422 adjoining said floating gate 406; and

a control gate 424 adjoining said ONO layer 422.

Regarding claim 22, Huang discloses the flash memory cell wherein said first silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 2, lines 9-16.

Regarding claim 23, Huang discloses the flash memory cell wherein said second silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 2, lines 9-16; col. 3, line 64 to col. 4, line 13.

Regarding claim 24, Huang discloses the flash memory cell wherein said dielectric material comprises a metal oxide. See col. 2, lines 9-16; col. 3, line 64 to col. 4, line 13.

Regarding claim 25, Huang discloses the flash memory cell wherein said dielectric layer comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 2, lines 9-16; col. 3, line 64 to col. 4, line 13.

Conclusion

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
December 11, 2005